



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:
Harry Q. Pon

Serial No.: 09/836,973

Filed: April 18, 2001

For: EMI and Noise Shielding for Multi-
Metal Layer High Frequency
Integrated Circuit Processes

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Art Unit: 2823

Examiner: Deven Collins

Atty Docket: ITL.0452US
P9563

Commissioner for Patents
Washington, D.C. 20231

2823
#5
Response

D. Smalls Logan

1-28-03

TECHNOLOGY CENTER 2800

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In response to the Office Action mailed December 4, 2002, the Applicant requests the Examiner to please consider the following remarks as follows:

REMARKS

Claims 13-15, 18, 20-21, 24, and 26-29 were rejected under 35 U.S.C. § 102(b) as anticipated by *Pan et al.* (U.S. Pat. No. 6,051,869).

Independent claim 13 recites an integrated circuit having a semiconductor substrate, an interconnection layer positioned over said substrate, a passive circuit element between said substrate and said interconnection layer, and a *trench that encircles said passive circuit element, said trench filled with a conductive material.*

The Applicant requests reconsideration and withdrawal of the rejection of claim 13 under 35 U.S.C. § 102(b) because *Pan* fails to teach or suggest an integrated circuit having a *trench that encircles said passive circuit element, said trench filled with a conductive material.*

Pan describes an integrated circuit and method for making it. The integrated circuit includes an *insulating layer, formed within a trench* that separates conductive elements of a conductive layer. (See, col. 3, line 14 – col. 4, line 10). Unlike the trench described in independent claim 13, the integrated circuit described by *Pan* does not have a *trench that encircles said passive circuit element, said trench filled with a conductive material.* The trench described by *Pan* is filled with an insulating material, rather than a conductive material.

Date of Deposit: JANUARY 15, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **First Class Mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, Washington, D.C. 20231.
Ella Sisco
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